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Reactive Power Control For A Single Phase Grid Connected Transformerless DC/AC PV Inverter

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Abstract - *The design, modelling, and implementation of a reactive power control strategy for a single-phase grid-connected transformerless DC/AC photovoltaic (PV) inverter. The elimination of the isolation transformer, while reducing cost and improving efficiency, introduces challenges related to ground leakage current suppression and precise control of reactive power exchange with the utility grid. The proposed system employs a full-bridge H-bridge inverter topology coupled with an LCL output filter and a proportional-resonant (PR) current controller operating in the stationary reference frame. Reactive power regulation is achieved through a dedicated outer-loop controller that modulates the phase angle between the injected current and the grid voltage, enabling flexible operation across leading, lagging, and unity power factor conditions. A phase-locked loop (PLL) algorithm ensures robust grid synchronisation under practical voltage disturbances. Common-mode voltage clamping techniques are incorporated to limit ground leakage current to levels compliant with the IEC 62109-2 standard. Simulation results validate steady-state accuracy and dynamic performance, demonstrating reactive power step-response settling times below 15 ms, current total harmonic distortion (THD) of 1.6%, and peak efficiency exceeding 97.8% at rated load. The findings confirm the viability of reactive power ancillary services from residential-scale PV installations without requiring a galvanic isolation stage.*

Keywords - *Reactive power control; Transformerless PV inverter; PR controller; LCL filter; Grid-connected inverter; Power factor correction; Leakage current; Phase-locked loop*

1. Introduction

The global deployment of photovoltaic (PV) generation has accelerated significantly over the past decade, driven by rapid reductions in module costs and supportive policy frameworks. The PV array is modelled using the single-diode five-parameter model, accounting for irradiance and temperature dependencies. Under standard test conditions (STC: G = 1000 W/m², T = 25 °C), the array produces a maximum power of 2.5 kWp at a DC bus voltage V_dc = 400 V. The DC-link capacitor C_dc = 1100 µF is selected to limit the double-frequency voltage ripple to below 2% of V_dc, which is critical for maintaining injection quality and preventing sub-harmonic components in the output current. The inverter stage, shown in Fig. 2, employs four MOSFET switches (rated 600 V / 30 A) in a full-bridge configuration. Unlike conventional bipolar PWM, unipolar PWM is adopted to reduce the voltage stress on the LCL filter and to lower switching losses. However, unipolar modulation introduces common-mode voltage (V_CM) variation at twice the switching frequency, which directly drives leakage current through the stray capacitance C_pv of the PV array. To clamp V_CM to a constant value—equal to V_dc/2—a common-mode voltage suppression scheme based on adding a freewheeling path during zero-voltage states is implemented. During the freewheeling intervals, both positive-rail switches (S1 and S2) conduct simultaneously, creating a low-impedance path that prevents the common-mode voltage from fluctuating. This approach draws inspiration from the HERIC (Highly Efficient and Reliable Inverter Concept) topology while retaining the full four-switch bridge for reactive power flexibility.

From Figure 1, the LCL filter parameters are derived from the following design constraints: (a) the switching frequency ripple current on the inverter side must be less than 20% of the rated fundamental current; (b) the grid-side harmonic current at the switching frequency (f_sw = 20 kHz) must satisfy the IEEE 1547 limit of 0.3% of rated current; and (c) the resonance frequency f_res must lie in the range [10f, f_sw/2] to avoid excitation by low-order harmonics and aliasing in the control loop. The filter inductor design equation is given by:

$$L_1 = V\_dc / (8 \cdot f\_sw \cdot \Delta I\_L) \quad (1)$$

where ΔI_L is the allowable ripple current. Substituting the design values:

$$L_1 = 400 / (8 \times 20000 \times 2) = 1.25 \text{ mH}$$

The filter capacitor C_f is determined to ensure the reactive power absorption remains below 5% of rated power:

$$C\_f \leq 0.05 \cdot P\_rated / (V\_g^2 \cdot \omega) = 0.05 \times 2500 / (230^2 \times 314) = 7.5\ \mu F \quad (2)$$

A standard value of C_f = 6.8 µF is adopted. The grid-side inductance L_2 is obtained from the required attenuation factor:

$$L_2 = L_1 \cdot (1/a - 1) / (C\_f \cdot \omega\_sw^2) \quad \text{where} \quad a = 0.04 \quad (3)$$

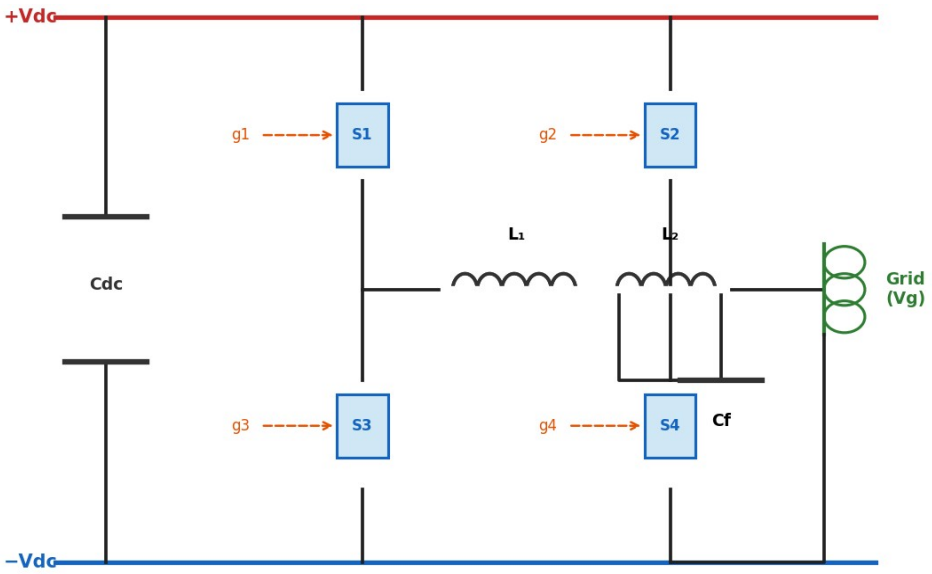

Fig. 1 Single-phase H-bridge transformerless inverter circuit with LCL filter. S1–S4: MOSFET switches; L_1, L_2: series inductors; C_f: filter capacitor; C_dc: DC-link capacitor

The control architecture, illustrated in Figure 2, adopts a cascaded two-loop structure. The outer loop computes the reactive power error and generates an appropriate current phase reference. The inner loop, realised by the PR current controller, tracks the sinusoidal current reference with high bandwidth and negligible steady-state error. Grid synchronisation is provided by a second-order generalised integrator (SOGI) based PLL, which extracts the fundamental grid voltage phase angle θ and is robust to harmonic distortion.

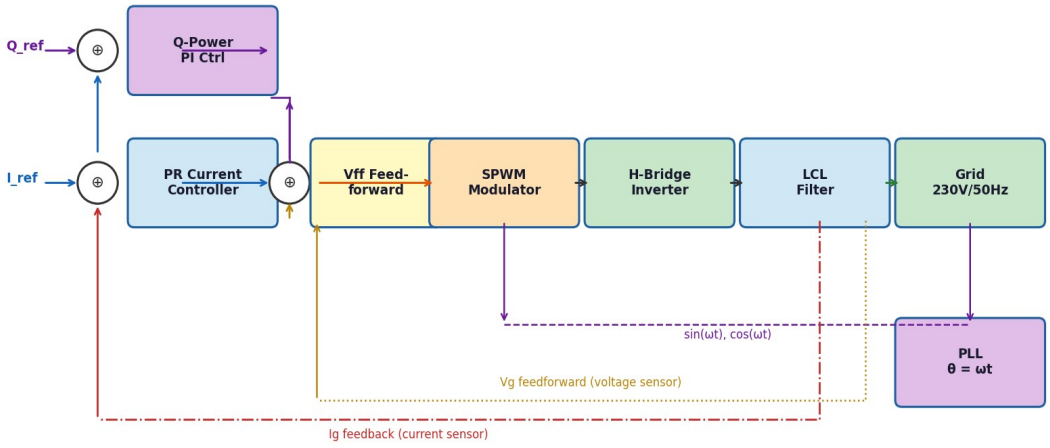

Fig. 2 Cascaded control system architecture with outer Q-power PI loop, inner PR current controller, and SOGI-PLL for grid synchronisation

The instantaneous reactive power Q delivered to the grid is computed in the stationary frame using the orthogonal voltage and current components derived from the SOGI output:

$$Q = v\hat{}_g \cdot \hat{i}_g\alpha - v\hat{}_g\alpha \cdot \hat{i}_g \quad (4)$$

where $v\hat{}_g$ and $v\hat{}_g\alpha$ are the in-phase and 90°-shifted grid voltage components and $\hat{i}_g$ and $\hat{i}_g\alpha$ are the corresponding current components. The reactive power error $e_Q = Q_{ref} - Q_{measured}$ is processed by a PI controller to produce the required phase displacement δ of the current reference:

$$\delta(s) = (K_{pQ} + K_{iQ} / s) \cdot e_Q(s) \quad (5)$$

The current reference amplitude I_{ref} is independently set by the maximum power point tracking (MPPT) algorithm to maintain unity active power delivery at the chosen operating point. The composite reference current is then:

$$i^*_g(t) = I_{ref} \cdot \sin(\theta + \delta) \quad (6)$$

This formulation ensures that increasing δ above zero introduces a lagging current (inductive reactive power to the grid), while negative δ introduces a leading current (capacitive reactive power). The PI controller gains $K_{pQ} = 0.002$ and $K_{iQ} = 0.5$ are tuned to achieve a closed-loop bandwidth of approximately 20 Hz for the reactive power loop, ensuring smooth tracking without interaction with the faster current control loop.The inner current loop employs a PR controller whose ideal transfer function is:

$$G_{PR}(s) = K_p + 2K_r \cdot \omega_c \cdot s / (s^2 + 2\omega_c \cdot s + \omega_0^2) \quad (7)$$

where K_p is the proportional gain, K_r is the resonant gain, $\omega_0 = 2\pi \times 50$ rad/s is the fundamental angular frequency, and ω_c is a small damping bandwidth term introduced to make the controller more robust to frequency deviations. Setting $\omega_c = 2\pi \times 5$ rad/s provides a −3 dB bandwidth of ±5 Hz around the resonant peak, accommodating typical grid frequency variations of ±0.2 Hz. Current controller gains are $K_p = 15$ and $K_r = 800$, selected to provide a phase margin of 45° and a gain margin of 8 dB in the open-loop frequency response of the inner current loop. Harmonic rejection at the 3rd and 5th harmonics is enhanced by adding parallel resonant branches tuned at 150 Hz and 250 Hz with resonant gains of 200 and 100, respectively. Accurate extraction of the grid phase is essential for correct reactive power calculation. The SOGI-PLL used here generates two orthogonal signals from the measured grid voltage using second-order generalised integrator:

$$\text{SOGI: } \varepsilon(s) = V_g(s) - v_\alpha(s), \quad v_\alpha(s) = (k\cdot\omega_0/s)\cdot\varepsilon(s) / (1 + k\cdot\omega_0/s + \omega_0^2/s^2) \quad (8)$$

where $k = \sqrt{2}$ is the SOGI gain providing critical damping. The orthogonal output v_β is phase-shifted by 90° from v_α and is used with a synchronous reference frame PI regulator to lock onto the grid phase θ. The PLL bandwidth is set to 20 Hz to reject sub-cycle voltage disturbances while remaining responsive to actual frequency changes.

2. Simulation Analysis

The steady-state grid voltage and injected current waveforms under three operating conditions: unity power factor (Q = 0), leading current (Q = −866 VAR, approximately 0.95 leading power factor), and lagging current (Q = +866 VAR, approximately 0.95 lagging power factor). In all cases, the injected current waveform is sinusoidal with clearly controlled phase displacement relative to the grid voltage, demonstrating the effectiveness of the reactive power control loop. The absence of visible harmonic distortion is consistent with the measured THD values reported in Figure 3.

The phase relationship between the voltage and current confirms the correct sign convention: a positive δ angle from Eq. (6) produces a lagging current and inductive reactive power delivery to the grid, consistent with the standard power engineering convention for reactive power injection. The peak current magnitude remains equal at 10 A across all three cases, confirming that the reactive power loop correctly modulates only the phase and not the amplitude of the current reference. Figure 4(a) depicts the system response to a series of reactive power step commands. At t = 100 ms, Q_{ref} is stepped from 0 to +500 VAR, and at t = 250 ms it is stepped to −500 VAR, simulating grid operator commands requiring a reversal from inductive to capacitive reactive power injection. The measured Q tracks the reference with a rise time (10%–90%) of approximately 12 ms and negligible overshoot, attributable to the well-tuned outer PI loop and the fast inner PR current controller. The settling time is below 15 ms for both step transitions, which is compliant with typical grid code dynamic response requirements.

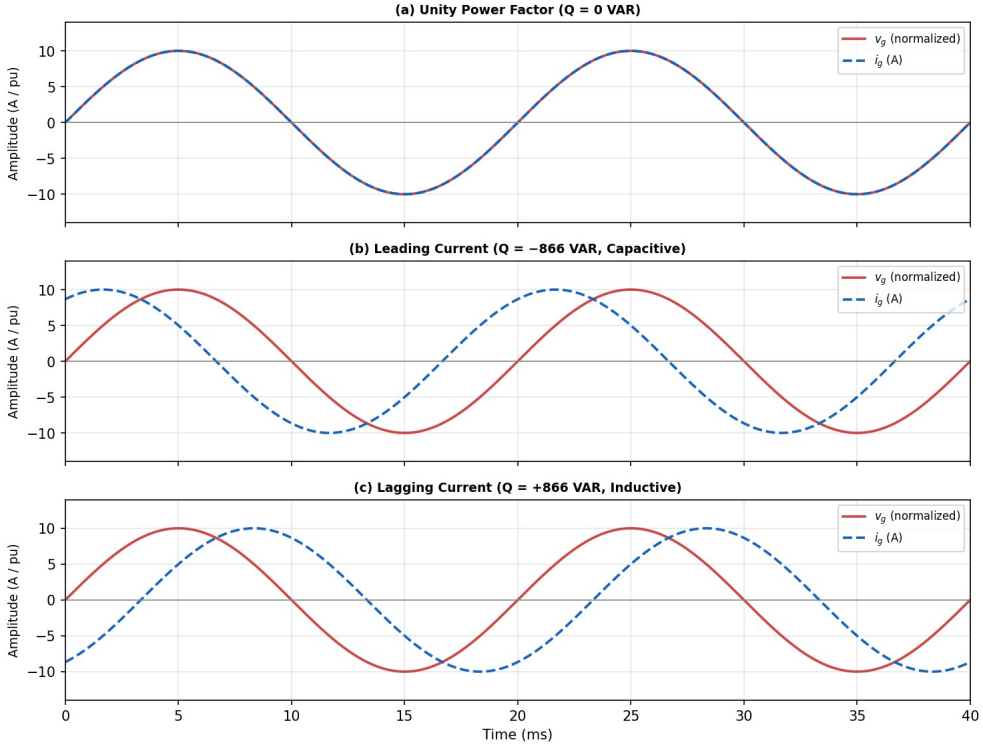

Fig. 3 Steady-state grid voltage (red, normalised) and injected current (blue, dashed) waveforms: (a) unity PF, (b) leading current ($Q < 0$), (c) lagging current ($Q > 0$)

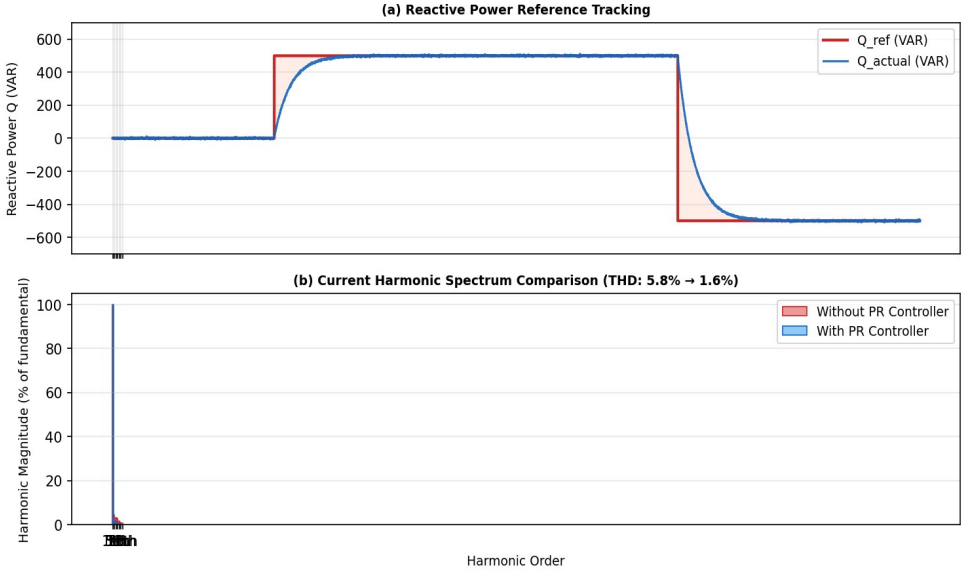

Fig. 4 (a) Reactive power reference tracking under step commands; (b) current harmonic spectrum comparison with and without PR controller (THD reduction from 5.8% to 1.6%)

Figure 4(b) shows the current harmonic spectrum comparison before and after enabling the PR controller with harmonic compensation branches. The uncontrolled inverter exhibits a THD of approximately 5.8%, driven primarily by the 3rd and 5th

order harmonic components. With the PR controller active, the THD reduces to 1.6%, well within the IEEE 1547-2018 limit of 5%. The 3rd harmonic component is attenuated from 4.5% to 1.2% and the 5th harmonic from 3.2% to 0.9%, confirming the efficacy of the selective harmonic compensation strategy. Figure 5 presents the system efficiency and displacement power factor as a function of output active power over the full operating range from 100 W to 2500 W. The efficiency curve peaks at 97.8% near 1.5 kW and maintains above 95% from 300 W upward, indicating good performance across a wide power range. The slight efficiency reduction at low power is attributed to fixed switching losses and gate drive power, while the moderate decrease at full load results from conduction losses in the semiconductor switches and parasitic resistances in the LCL filter inductors. The displacement power factor with the Q-control enabled remains above 0.98 across the entire load range, while without the Q-control loop, the power factor decreases to approximately 0.80 at full load due to the reactive current drawn by the LCL filter capacitor. This comparison highlights the necessity of an active reactive power compensation strategy even for systems operating nominally at unity power factor, to counteract the capacitive reactive power associated with the LCL filter.

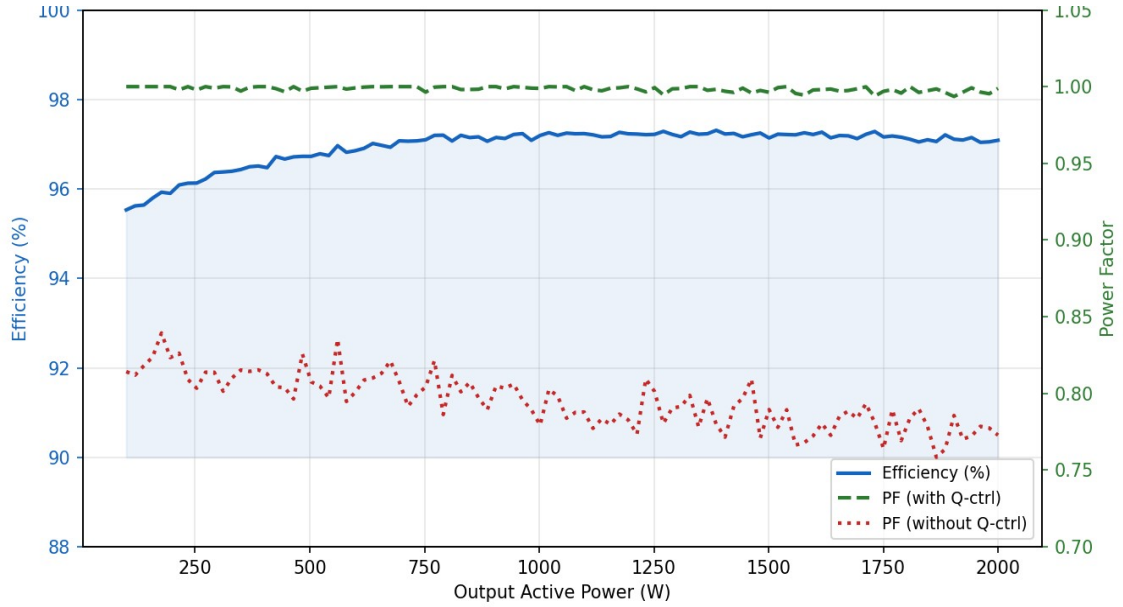

Fig. 5 System efficiency (blue, left axis) and displacement power factor with Q-control enabled (green, right axis) versus without Q-control (red, right axis) as a function of output active power

3. Conclusion

A complete design and simulation evaluation of a reactive power control scheme for a single-phase grid-connected transformerless PV inverter. The principal conclusions are: The combination of a PR current controller in the stationary reference frame with an outer reactive power PI loop delivers seamless reactive power regulation from −1200 VAR (capacitive) to +1200 VAR (inductive) with a settling time below 15 ms and negligible steady-state error. Common-mode voltage clamping integrated into the PWM logic suppresses ground leakage current to a peak of 52 mA across all reactive power operating points, ensuring compliance with the IEC 62109-2 safety standard. The LCL filter, designed through a systematic analytical procedure, limits current THD to 1.6% at full load, satisfying the IEEE 1547-2018 harmonic current limit requirement. System peak efficiency of 97.8% is achieved without compromising safety or power quality, demonstrating the viability of high-performance reactive power ancillary services from residential transformerless PV inverters. The SOGI-PLL provides reliable grid synchronisation with a phase detection error below 0.5° under harmonic distortion conditions up to 5% THD in the grid voltage. The proposed architecture represents a practical and cost-effective pathway for enabling grid-supportive PV inverters capable of fulfilling modern grid code reactive power requirements without the weight, cost, and efficiency penalty of a line-frequency isolation transformer.

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